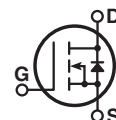
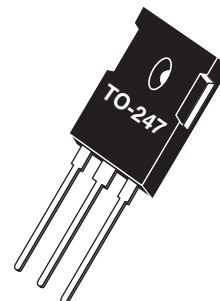


POWER MOS V®

APT20M45BVR(G)

POWER MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increase packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.


FEATURES

- Faster switching
- Lower Leakage
- 100% Avalanche tested
- Popular TO-247 Package
- RoHS compliant 

Absolute Maximum Ratings

 All Ratings: $T_c = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain Source Voltage	200	Volts
I_D	Continuous Drain Current @ $T_c = 25^\circ\text{C}$	56	Amps
I_{DM}	Pulsed Drain Current ¹	224	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_c = 25^\circ\text{C}$	300	Watts
	Linear Derating Factor	2.4	W/C°
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature for Soldering: 0.063" from Case for 10 Seconds	300	
I_{AR}	Avalanche Current ¹ (Repetitive and Non-Repetitive)	56	Amps
E_{AR}	Repetitive Avalanche Energy ¹	30	mJ
E_{AS}	Single Pulse Avalanche Energy ⁴	1300	

Static Characteristics
 $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	200			Volts
$I_{D(on)}$	On State Drain Current ² ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	56			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ² ($V_{GS} = 10V, 0.5 I_{D(Cont.)}$)			0.045	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			25	μA
	Zero Gate Voltage Collector Current ($V_{GS} = 0.8 V_{DSS}, V_{GS} = 0V, T_c = 125^\circ\text{C}$)			250	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1.0mA$)	2		4	Volts


CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

Dynamic Characteristics

APT20M45BVR(G)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
C_{iss}	Input Capacitance	$V_{GS} = 0V$		4050	4860	pF
C_{oss}	Output Capacitance	$V_{DS} = 25V$		980	1375	
C_{rss}	Reverse Transfer Capacitance	$f = 1MHz$		300	450	
Q_g	Total Gate Charge ¹	$V_{GS} = 10V$		130	195	nC
Q_{ge}	Gate-Source Charge	$V_{DD} = 0.5V_{DSS}$		30	45	
Q_{gd}	Gate- Drain ("Miller") Charge	$I_D = I_{D(cont.)} @ 25^\circ C$		55	80	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 10V$		12	24	ns
t_r	Rise Time	$V_{DD} = 0.5V_{DSS}$		14	28	
$t_{d(off)}$	Turn-off Delay Time	$I_D = I_{D(cont.)} @ 25^\circ C$		43	70	
t_f	Fall Time	$R_G = 1.6\Omega$		7	14	

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic / Test Conditions	Min	Typ	Max	Unit
I_S	Continuous Source Current (Body Diode)			56	Amps
I_{SM}	Pulse Source Current ¹ (Body Diode)			224	
V_{SD}	Diode Forward Voltage ² ($V_{GS} = 0V$, $I_S = -I_{D(cont.)}$)			1.3	Volts
t_{rr}	Reverse Recovery Time ($I_S = -I_{D(cont.)}$, $dI_S/dt = 100A/\mu s$)		280		nS
Q_{rr}	Reverse Recovery Time ($I_S = -I_{D(cont.)}$, $dI_S/dt = 100A/\mu s$)		3.5		μC

Thermal Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
$R_{\theta JC}$	Junction to Case			0.42	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

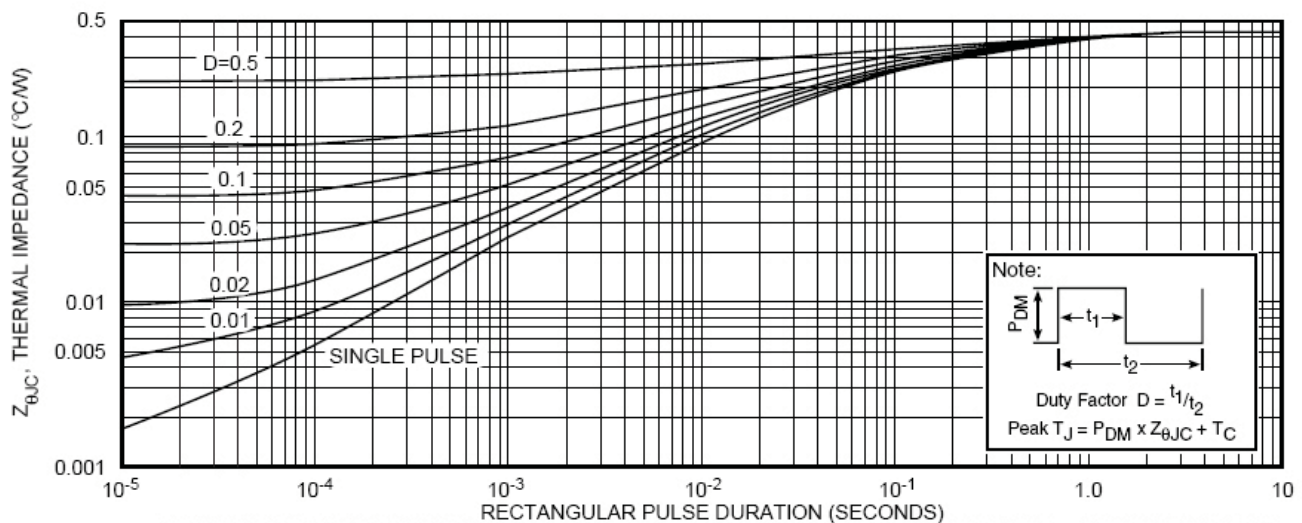
① Repetitive Rating: Pulse width limited by maximum junction temperature.

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

Microsemi Reserves the right to change, without notice, the specifications and information contained herein.

③ See MIL-STD-750 Method 3471

④ Starting $T_J = +25^\circ C$, $L = 830\mu H$, $R_G = 25\Omega$, Peak $I_L = 56A$



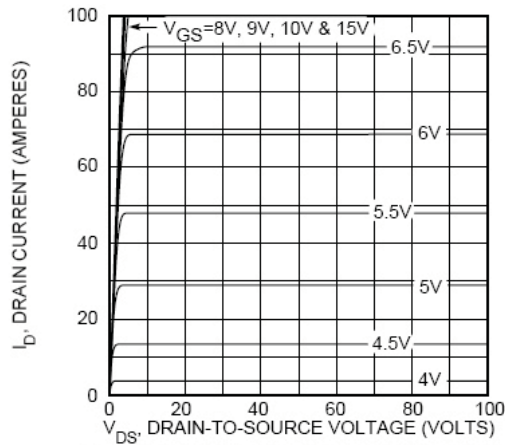


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

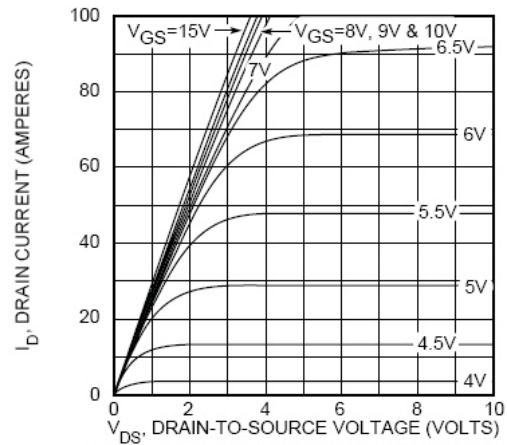


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

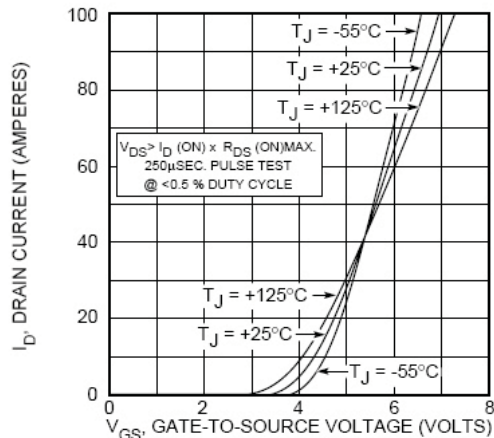


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

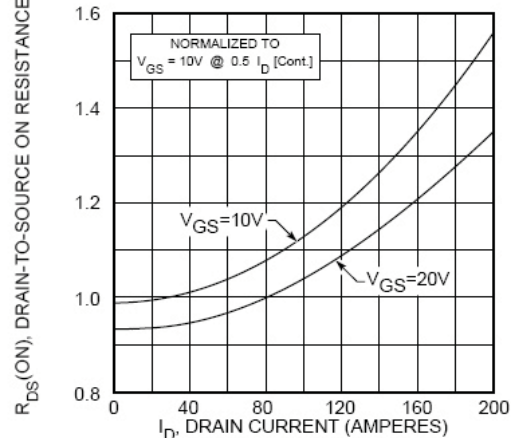


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

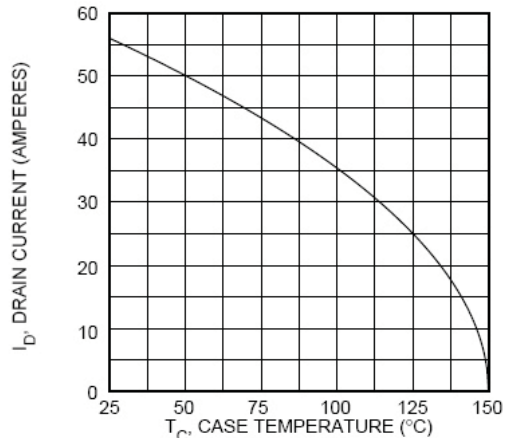


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

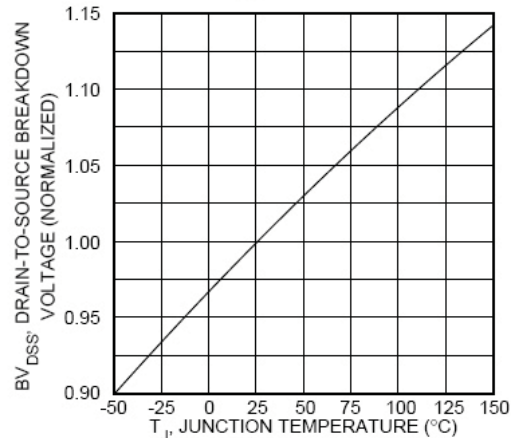


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

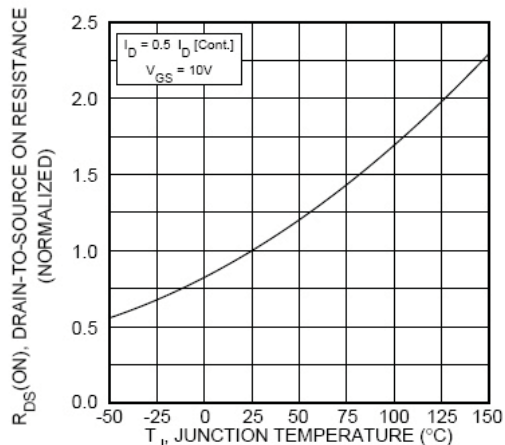


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

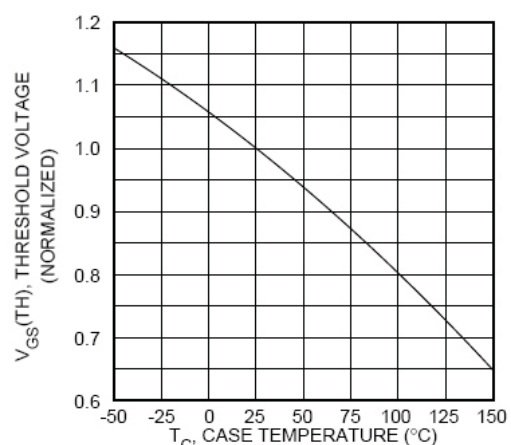


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

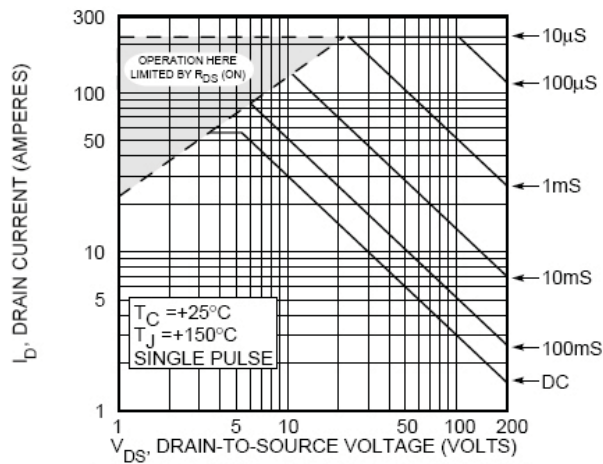


FIGURE 10, MAXIMUM SAFE OPERATING AREA

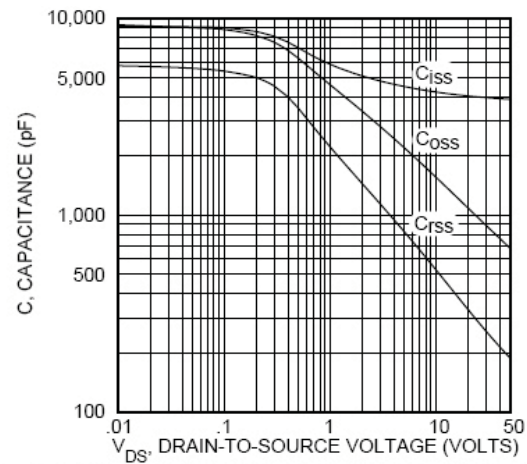


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

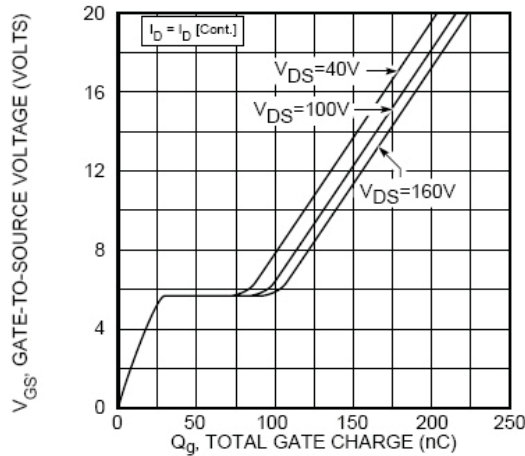


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

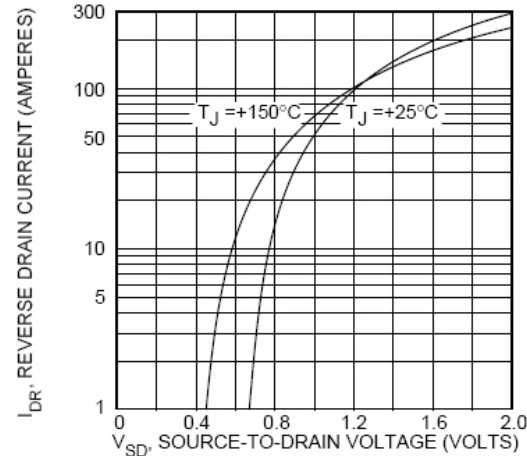
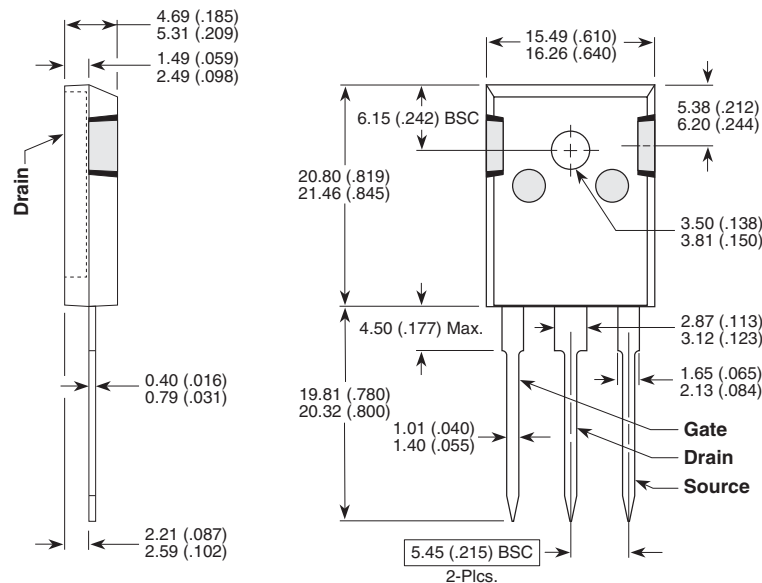


FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-247 (B) Package Outline

e3 100% Sn Plated



Dimensions in Millimeters and (Inches)

Microsemi's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 6,939,743, 7,352,045 5,283,201 5,801,417 5,648,283 7,196,634 6,664,594 7,157,886 6,939,743 7,342,262 and foreign patents. US and Foreign patents pending. All Rights Reserved.